FB4CGG5@VU09P TimeSync

Quad QSFP28 port card supporting 4x100GE, 16xPCIe Gen3, AMD® Virtex Ultrascale+ V09P

Product Description

The FB4CGG5@VU09P TimeSync is a high-performance OEM hardware platform intended for 10/40/25/100 Gigabit Ethernet via its quad QSFP28 slots.

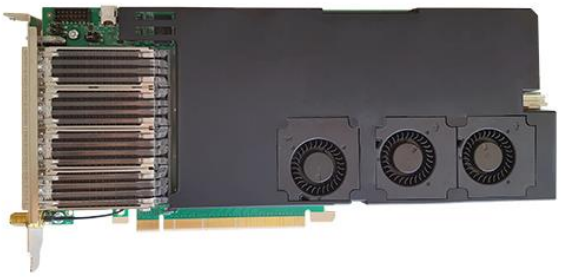
The card supports various FPGA models, and in its standard version it is fitted with an AMD® Virtex UltraScale+ VU9P FPGA SG3, to provide ample capacity for the quad QSFP28 interface.

The card is mounted with 2 x 64-bit DDR4 2400MT/s 4GB for a total of 8 GB. In addition to this it features 2 SODIMM sockets for use with DDR4 or QDRII+ modules for low latency applications.

The card features the ZL30793 DPLL for optimal clock control, allowing compliance with IEEE-1588-2019 SyncE and PTP.

Key Features

- AMD® Virtex UltraScale+ VU9P FPGA
- 4 x QSFP28 ports
- DPLL ZL30793
- 2 x 64-bit DDR4@2400MT/s
- 2 x SODIMM for optional QDRII+ or extra DDR4
- Configuration flash RAM for boot images
- PCIe form-factor: 3/4 length, standard height PCIe
- On-board power and temperature sensors
- FPGA controlled link and status LEDs
- Passive cooling (optional)



Technical Specifications

Network Interface	
IEEE standard:	IEEE 802.3 10/40/25/100 GE
Interfaces:	• Physical interface: 4 x QSFP28 ports (2 port variant available) • Supported QSFP+/QSFP28 modules: including fan-out • modules for 4x10G/4x25GE, Multimode SR4 (850nm), • singlemode LR4 (1310nm), multimode LRM4 (1310nm), or Direct Attached Copper (Twinax) and others. • Data rate: 16×10, 4×40, 16×25, 4×100 Gbps
Host Interface	
PCI bus:	• Physical bus connector: 16-lane PCIe • PCIe bus type: 1-16 lane PCIe Gen1/Gen2/Gen3 via on-board PLX PCIe switch. • Optional 2×8 PCIe lanes via secondary High speed serial connector
General Technical Specifications	
Configuration:	• 16-bit fast parallel programming interface from supporting preprogrammed controller • Configuration flash supports two boot images with automatic fallback to fail safe image if first image fails • Upload of FPGA configuration to flash via PCIe • Support for encrypted FPGA bit file (optional)
On-board Memory:	• 2 x 64-bit DDR4@2400MT/s 4 GB • 2 x Optional SODIMM • – 64-bit DDR4@2400MT/s 4 GB • 8 MB user configurable space in flash for permanent storage
On-board Clock:	• PCIe clock: 100 MHz • 200 MHz clock • 50 MHz clock • 161.13 MHz clock • DPLL ZL30793
FPGA Details:	• AMD® Virtex Ultrascale+ XCVU9P

Environment:	• Physical dimensions: 3/4 length, standard height PCIe • Power consumption: Operating temperature: 0 – 55°C, 30 – 130°F • Operating humidity: 20 – 80% • Hardware compliance: RoHS, CE • Active cooling (heat sink with fan) • Passive cooling (optional)
Time Synchronization:	• PTP: Yes, with PTP4L or zlsptp on x86 • Support Sync-E/ 1588 standard • DPLL: ZL30793
Additional Intellectual Property Modules:	• PacketMover framework (optional) • SmartNIC framework (optional) • Ultra low latency 10GE MAC (optional) • TCP-offload engine (optional)