Silicom Connectivity Solutions

FPGA SmartNIC N6010/6011 Intel based

Flexible Multi-port Ethernet Intel® AgileX Based SmartNIC

Product Description

The Silicom FPGA SmartNIC N6010/N6011 is a high-performance OEM hardware platform intended for hardware acceleration for mobile 4G and 5G Baseband Units or Distributed Units with two QSFP28 modules. Example: supports up to 4 100MHz carriers Radio Units via 4x 25G eCPRI/CPRI with SFP28 modules, as well as interfacing to a Grand master via QSFP28 at 10/25G.

The card is based on an Intel® AgileX AGF014, which embeds a Hard Processor System (HPS) with four 64-bit Application Processing Units (ARM Cortex-A53) along with a powerful Programmable Logic part.

The design is set to work in ORAN LLS-C1 and C2 with the intention to be utilized with a 4G/5G IP stack interfacing at 3GPP functional split options 6 for CPRI or 7.2x for eCPRI.

The Silicom FPGA SmartNIC N6011 is supported by the Intel® Open FPGA Stack (OFS). The Intel OFS FPGA Interface Manager (FIM) provides a common developer interface to both application and acceleration function developers and includes drivers, Application Programming Interfaces (APIs) and an FPGA factory image.

Silicom validates each FPGA SmartNIC N6011 to support large scale deployments requiring FPGA acceleration. This OEM accelerator card is targeted for Intel® Xeon-SP and Intel® Xeon-D systems.

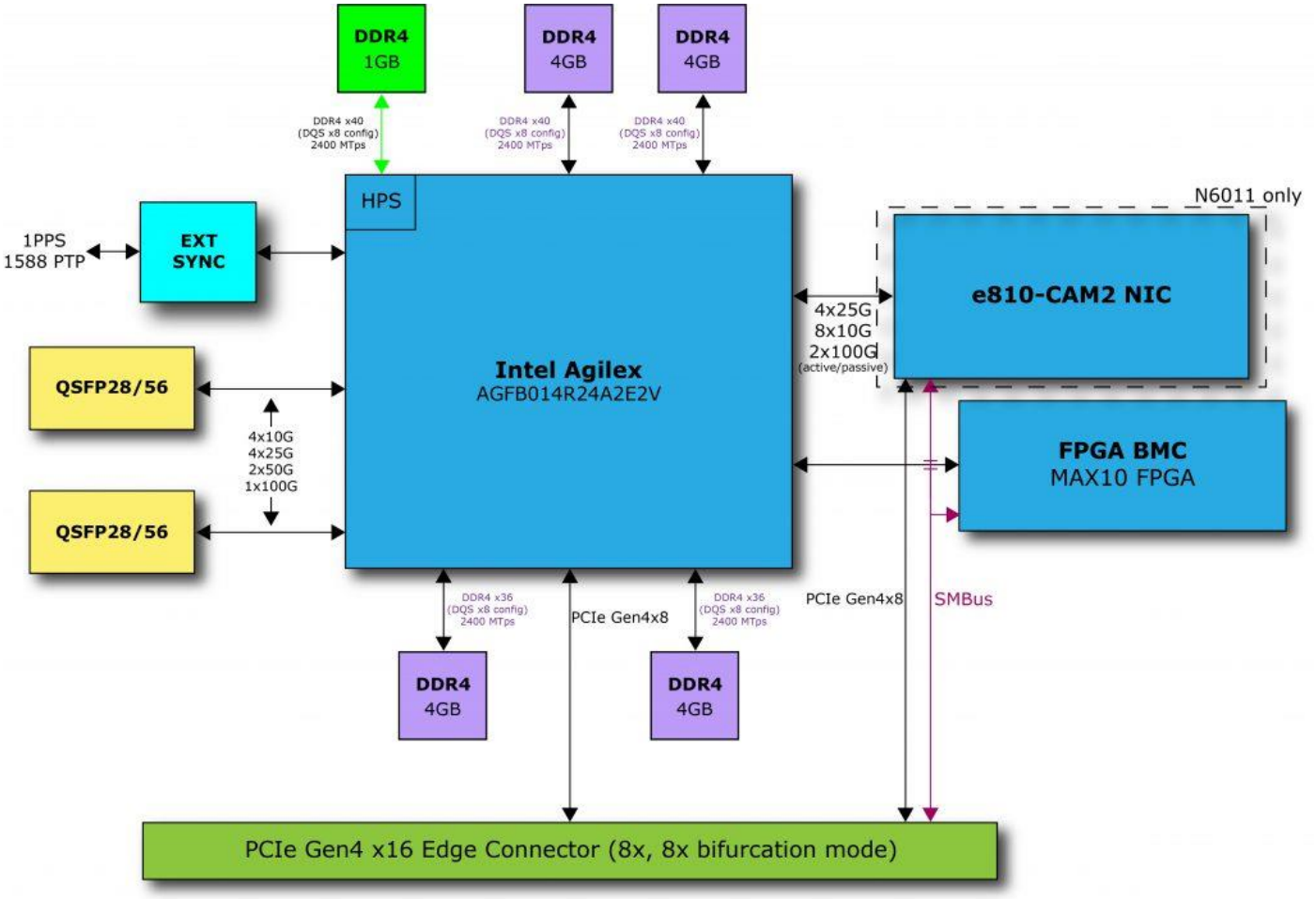
The Silicom FPGA SmartNic platform is targeted for market-specific acceleration in applications listed below:

Silicom FPGA N6010/6011 Use Cases:

- 4G/5G vRAN Acceleration
- Network Function Virtualization (NFV)
- Multi-Access Edge Computing (MEC)
- Video Transcoding
- Cyber Security
- High-Performance Computing
- Finance

Key Features

- Intel® Agilex® FPGA
- Intel® e810-CAM2 NIC
- 2 x 100 GbE/4 x 25GbE/8 x 10GbE
- PCIe v4 x 8 (x16 physical)



Technical Specifications

Network Interface:	
IEEE standard	• IEEE 802.3 10GE, 25GE, 100GE
Interfaces	• Physical interface: 2 x QSFP28/56 slots • Supports QSFP28/56 modules with Multimode SR (850nm), single mode LR (1310nm), multimode LRM (1310 nm) • Data rate: Each module 100G, 4x25G, 4x10G • Support for SyncE
Interfaces:	

Network	• 2x100GbE, using QSFP28/56
Host	• PCIe 4.0 x 16 (N6011 is bifurcated x8, x8) • NCSI RBT • Support for SMBUS
General Technical Specifications:	
NIC details	**Intel® E810-CAM2** • Interfaces to PCIe 4.0 x8 • Supports 2x100GE (active/protect), 4x25GE and 8x10GE
FPGA Details	**Intel® Agilex™ AGF014** • 1.4M Logic Element Fabric • Provides Ethernet or Ethernet and Common Public Radio Interface (CPRI) interface over QSFP28/56 ports • P-Tile – Provides PCIe Gen4 x8 interface to the host • Hard Processor System (HPS) • DDR4 Memory controllers interfacing to the FPGA fabric • Platform Management Communications Interface (PMCI) module
Configuration	• Configuration flash can be made to support multiple boot images for automatic fallback to factory default image • Upload of FPGA configuration to flash via PCIe • Direct FPGA configuration via the onboard JTAG dongle
On-board Memory	• 8 GB DDR4 memory, with ECC (2 channels) • 8 GB DDR4 memory, without ECC (2 channels) • 1 GB DDR4 memory for HPS • 280 MB Flash memory for non-volatile storage
On-board Clock	• PCIe clock: 100 MHz • 8 output reprogrammable clock generator • Supports network synchronization
Additional Board Support	• On-board power and temperature sensors (via SMBus/I2C) • FPGA controlled Link and Activity LED for each port. 2 for each QSFP28 • Board status LEDs • FPGA Reset via host I2C
Environment	• Full height, ½ length 111.28 x 167.65 mm with bracket • Storage temperature: -40 – 65°C -40 – 149°F • Operating temperature (card inlet): -5 – 50°C, 23 – 122°F • Operating humidity: 5 – 85% • Hardware compliance: RoHS, FCC, CE

Power	• Max 125W, above 75W PCIe AUX power must be used • Passive cooling • Power and temperature monitoring via SMBus/I2C • PCIe AUX power connector available
Manageability Features	• Full card BMC solution host communication via SMBus (PLDM & NC-SI) • FPGA image remote update capability • Full security implementation using MAX10 FPGA as RoT
Networking	• A configurable packet processor IP core • Extensive configuration API • Packet forwarding and bridging across network, main host and SoC • Parsing, match and action operations • Bandwidth rate limit
Hardware Acceleration	• SR-IOV, 256 virtual functions • 32 physical functions
Software Support	• Open FPGA Stack (IOFS) • Contrail • OVS • SRv6 • vFW acceleration • 4G and 5G vRAN enablement package • DPDK • BBDev • FlexRAN

Order Information

P/N	Notes:
FB2CG2@AGF14-A1P2	Silicom FPGA SmartNIC N6011 (base + Intel NIC)
FB2CG1@AGF14-A0P2	Silicom FPGA SmartNIC N6010 (base)

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