

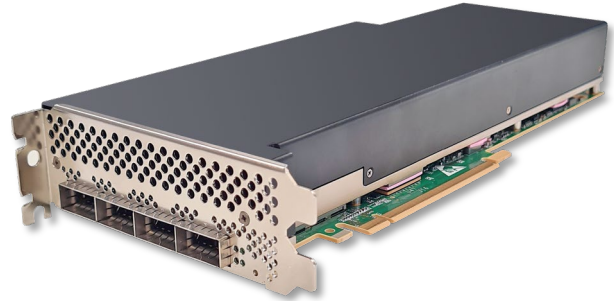


### Silicom FPGA SmartNIC N5013

Quad port QSFP28, 100 GE, PCIe Gen4 x16, Intel® Stratix® 10 DX FPGA Based, 8GB HBM2

#### Product Description

The FB4CGG2@S10D21 FPGA SmartNIC N5013 is a high-performance programmable PCIe Server adapter based on the Intel® Stratix® 10 DX 2100 FPGA. The Stratix 10 DX 2100 is an extremely powerful FPGA which also features on-chip 8GB HBM2 memory providing an unprecedented 512 GByte/s of total aggregate bandwidth.



#### Key Use Cases

- Network Function Virtualization (NFV)
- Multi-Access Edge Computing (MEC)
- Cyber Security
- High-Performance Computing
- Finance
- Mobile Access and Core Network



#### Key Features

- Intel® Stratix® 10 DX 2100 FPGA
- HBM2: 8GB (2x4 GB, internal)
- DDR4/ 32GByte+ECC (x18 devices)
- QDR-IV: 144Mbit
- PCIe x16 Gen4
- Intel® Max® 10 Board Management Controller
- On-board power and temperature sensors
- FPGA controlled link and status LEDs
- Time Synchronization via IEEE 1588 (PTP) and SyncE (optional)
- Optional external Sync bracket with 4 x SMA for in/out of PPS and 10MHz

## Technical Specifications

Network Interface	
IEEE standard	IEEE 802.3 100GbE, 40GbE, 25GbE, 10GbE
Interfaces	<ul style="list-style-type: none"> <li>Physical interface: 4 x QSFP28 slots</li> <li>Multimode SR4 (850nm), Single Mode LR4 (1310nm) or Direct Attached Copper (Twinax)</li> <li>Data rate: 4x100, 4x40, 16x25, 16x10 Gbps</li> </ul>
Host Interface	
PCI bus	<ul style="list-style-type: none"> <li>PCIe 4.0 x16</li> </ul>

General Technical Specifications	
FPGA Details	<b>Intel® Stratix® 10 DX 2100</b> <ul style="list-style-type: none"> <li>2.073M Logic Element Fabric</li> <li>HBM2: 8GB (2x4 GB, internal)</li> </ul>
Configuration	<ul style="list-style-type: none"> <li>Configuration flash can be made to support multiple boot images for automatic fallback to factory default image</li> <li>Upload of FPGA configuration to flash via PCIe – with supported image and tool</li> </ul>
On-board Memory	<ul style="list-style-type: none"> <li>DDR4, 32GB +ECC (x18 devices), 2 banks of 16G + ECC.</li> <li>QDR-IV XP, 144Mbit</li> <li>HBM2, 8GB in Stratix 10 DX2100</li> </ul>
On-board Clock	<ul style="list-style-type: none"> <li>PCIe clock: 100 MHz</li> <li>8 output reprogrammable clock generator</li> <li>Supports network synchronization</li> </ul>
Additional Board Support	<ul style="list-style-type: none"> <li>On-board power and temperature sensors (via SMBus/I2C)</li> <li>LEDs for board status and board management</li> </ul>
Physical Dimensions	<ul style="list-style-type: none"> <li>Full height, ¾ length, Dual Slot Passive</li> </ul>
Environment	<ul style="list-style-type: none"> <li>Storage temperature: -40°C–65°C (-40°F–149°F)</li> <li>Operating temperature: 0°C – 45°C (32°F – 113°F)</li> <li>Hardware compliance: RoHS, FCC Class A, CE, UL</li> </ul>
Thermal Design	<ul style="list-style-type: none"> <li>Passive heat sink targeted to dual slot</li> </ul>
Power	<ul style="list-style-type: none"> <li>Max 225W</li> <li>75W max from the PCIe Slot</li> <li>150W max from the 12V Aux 2x4 Connector</li> </ul>
Port LEDs	<ul style="list-style-type: none"> <li>4 x Link/ ACT for the 4 x QSFP28, on bracket</li> <li>1 x multi color status LED, on bracket</li> </ul>
Time Synchronization	<ul style="list-style-type: none"> <li>Support Sync-E/ 1588 standard (option for SW support)</li> <li>Bracket mounted SMA connector, optional</li> <li>Support for external Sync bracket with 4 x SMA for in/out of PPS and 10MHz</li> </ul>
Board Management	<ul style="list-style-type: none"> <li>Intel® Max® 10 FPGA Board Management Controller</li> <li>Voltage level monitoring</li> <li>Thermal shut-down protection</li> <li>Over current protection on 12V input</li> </ul>

## Ordering Information

Product Line	Ordering P/N	Notes
N5013	<b>FB4CGG2@S10D21-D00P0</b>	0: (0) E810-CAM1 0: $\frac{3}{4}$ Length, 10" P: Passive heat sink, dual slot 0: No external Sync bracket
N5013	<b>FB4CGG2@S10D21-D00P1</b>	0: (0) E810-CAM1 0: $\frac{3}{4}$ Length, 10" P: Passive heat sink, dual slot 1: With external Sync bracket

V1.2