



### Silicom C5010X Data Center NIC

#### Product Description

Silicom C5010X is an advanced data processing network interface controller, featuring cutting edge I/O and data processing capabilities, optimized for virtualized cloud, cloud native or bare metal virtualization. Completely implementing I/O workload using industry standard interfaces, Silicom C5010X is operated using stock virtio and NVMe drivers, implementing a true hardware virtio and NVMe PCIe interface. Combining two powerful engines – Intel® Stratix® 10 DX 1100 FPGA and Intel® Xeon® D-1612 SoC (x86 CPU, 4 cores, 8 threads) – Silicom C5010X data processing NIC brings together the power and flexibility of FPGA and the wealth of the x86 ecosystem.

A unique 3-way path for application optimization guarantees fast results. The presence of a x86 based CPU allows you to leverage existing software assets, where the FPGA flexibly enables extremely performant data path implementation:

- 1) In the first stage, the card can serve as a standard NIC with minimal configuration changes, with minimal orchestration modification;
- 2) Second stage include a migration of data plane and VM switching functionality from main host down to x86 CPU cores on card;
- 3) The third stage involves data path implementation on the FPGA.

Silicom C5010X can be deployed as a virtio network accelerator, a virtio storage accelerator, a NVMe storage (network) controller, a RDMA OFED controller, either separately or all at the same time. Further implementations such as flow filtering, encryption, compression, deduplication and machine learning, are facilitated by C5010X facilitates as complete infrastructure implementation on an NIC.

As the data path is implemented on the card, fewer risks and vulnerabilities are left to the cloud data center infrastructure.

Storage data paths in a cloud environment are often associated with the use of a storage attached network (SAN), serving the compute nodes over the network. The use of an x86 CPU core NIC with FPGA facilitates for allows relatively easy implementation of storage volume virtualizations, accessible on the host using stock storage software stacks, such as NVMe.

#### Key Use Cases

- Virtual Cloud
- Bare Metal Cloud
- NVFi
- Secure Infrastructure
- Cloud Storage

#### Key Features

- Intel® Xeon® D-1612 @ 1.5GHz 4 core, 8 threads
- Intel® Stratix® 10 DX 1100
- virtio-net and virtio-blk over PCIe
- Dual 25GbE
- PCIe v4 x 8 (x16 physical)

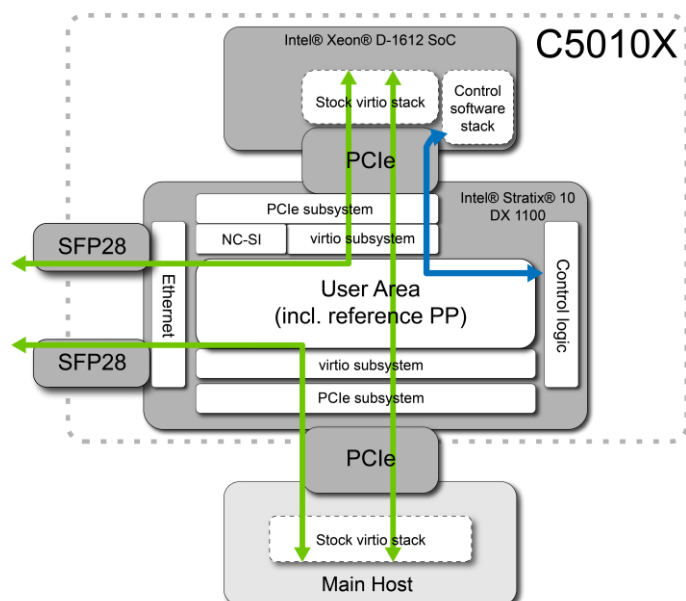


Figure 1 – Various data paths (green) and control paths (blue) are enabled on Silicom C5010X

## Technical Specifications

Network Interface	
IEEE standard	IEEE 802.3 10GE, 25GE
Interfaces	<ul style="list-style-type: none"> <li>Physical interface: 2 x SFP28 slots</li> <li>Supports SFP+/SFP28 modules with Multimode SR (850nm), single mode LR (1310nm), multimode LRM (1310 nm), or Direct Attached Copper (Twinax) and others</li> <li>Data rate: 2x10, 2x25, Gbps</li> <li>Support for SyncE</li> </ul>
Interfaces	
Network	<ul style="list-style-type: none"> <li>Dual 25GbE, using SFP28</li> </ul>
Host	<ul style="list-style-type: none"> <li>PCIe gen4 x 8 (x16 physical)</li> <li>NCSI RBT</li> <li>Support for SMBUS</li> </ul>
SoC	<ul style="list-style-type: none"> <li>PCIe v3 x 8</li> <li>USB NIC</li> <li>UART</li> </ul>

General Technical Specifications	
SoC details	<b>Intel® Xeon® D-1612</b> <ul style="list-style-type: none"> <li>4 x86 64 bit cores @1.5GHz</li> <li>8 threads</li> <li>6MB cache</li> <li>VT-d, VT-x</li> <li>Intel® AVX2</li> <li>AES-NI</li> <li>16GB DDR ECC</li> </ul>
FPGA Details	<b>Intel® Stratix 10 DX 1100</b> <ul style="list-style-type: none"> <li>Intel® Hyperflex™ core architecture</li> <li>Intel® Embedded Multi-die Interconnect Bridge (EMIB)</li> <li>PCIe Gen4 x16 hard IP, SRIOV</li> <li>Fixed point and IEEE 754 compliant floating-point variable precision digital signal processing (DSP) block</li> <li>Internal memory <ul style="list-style-type: none"> <li>M20K, 107Mb</li> <li>eSRAM, 47.25Mb</li> <li>MLAB</li> </ul> </li> <li>1,325,000 ALM</li> <li>Quad-core 64-bit Arm® Cortex®-A53 embedded processor @1.5 GHz</li> <li>4GB DDR</li> </ul>
Configuration	<ul style="list-style-type: none"> <li>Configuration flash can be made to support multiple boot images for automatic fallback to fail safe</li> <li>Upload of FPGA configuration to flash via PCIe</li> <li>Direct FPGA configuration via the onboard JTAG dongle</li> </ul>
On-board Memory	<ul style="list-style-type: none"> <li>16GB DDR ECC for SoC</li> <li>4GB DDR for FPGA</li> <li>User configurable space in flash RAM for permanent storage</li> <li>Configuration flash RAM for boot images</li> </ul>
On-board Clock	<ul style="list-style-type: none"> <li>PCIe clock: 100 MHz</li> <li>Core Clock 125Mhz</li> <li>2 x differential 312.5 MHz SerDes clock for Ethernet</li> <li>2 x differential 266.67 MHz/300MHz/333.33MHz clock for Memory</li> <li>Calibration clock 125MHz, 100MHz, 25MHz</li> <li>50 MHz clock</li> </ul>

<b>Additional Board Support</b>	<ul style="list-style-type: none"> <li>▪ On-board power and temperature sensors (via SMBus/I2C)</li> <li>▪ FPGA controlled Link and Activity LED for each port. 2 for each SFP28</li> <li>▪ Board status LEDs</li> <li>▪ FPGA Reset via host I2C</li> </ul>	
<b>Environment</b>	<ul style="list-style-type: none"> <li>▪ Full height, ½ length 111.15 x 167.65 mm with bracket</li> <li>▪ Storage temperature: -30 - 70°C -22 – 158°F</li> <li>▪ Operating temperature (card inlet): 0 – 55°C, 30 – 130°F</li> <li>▪ Operating humidity: 20 – 80%</li> <li>▪ Hardware compliance: RoHS, FCC, CE</li> </ul>	
<b>Power</b>	<ul style="list-style-type: none"> <li>▪ Max 75W</li> <li>▪ Passive cooling</li> <li>▪ Power and temperature monitoring via SMBus/I2C</li> </ul>	
<b>Management</b>	<ul style="list-style-type: none"> <li>▪ SoC boot options: PXE, SATA</li> <li>▪ SoC control interfaces: USB, UART, network</li> </ul>	
<b>Networking</b>	<ul style="list-style-type: none"> <li>▪ A configurable packet processor IP core</li> <li>▪ Extensive configuration API</li> <li>▪ Packet forwarding and bridging across network, main host and SoC</li> <li>▪ Parsing, match and action operations</li> <li>▪ Bandwidth rate limit</li> </ul>	
<b>Hardware Acceleration</b>	<ul style="list-style-type: none"> <li>▪ True hardware virtio interface</li> <li>▪ virtio 0.95</li> <li>▪ virtio 1.0</li> <li>▪ virtio – vDPA with live migration backend support</li> <li>▪ virtio-net backend over PCIe</li> <li>▪ virtio-blk backend over PCIe</li> <li>▪ virtio-iscsi (future)</li> <li>▪ NVMeoF</li> <li>▪ RDMA OFED</li> <li>▪ SR-IOV, 256 virtual functions</li> <li>▪ 32 physical functions</li> </ul>	
<b>Software Support</b>	<ul style="list-style-type: none"> <li>▪ DPDK</li> <li>▪ XDP</li> <li>▪ SPDK</li> <li>▪ OVS</li> <li>▪ KVM</li> <li>▪ VMWARE</li> <li>▪ OpenStack, Cinder client, Nova client</li> <li>▪ Ceph RBD</li> <li>▪ virtio 0.95</li> <li>▪ virtio 1.0</li> </ul>	<ul style="list-style-type: none"> <li>▪ virtio – vDPA</li> <li>▪ NVMeoF</li> <li>▪ NGINX</li> <li>▪ Squid</li> <li>▪ HAProxy</li> <li>▪ Snort</li> <li>▪ Suricata</li> <li>▪ Bro</li> <li>▪ Redis</li> </ul>

## Ordering Information

FB2XXVG@S10D11-HDNP

v1.0

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