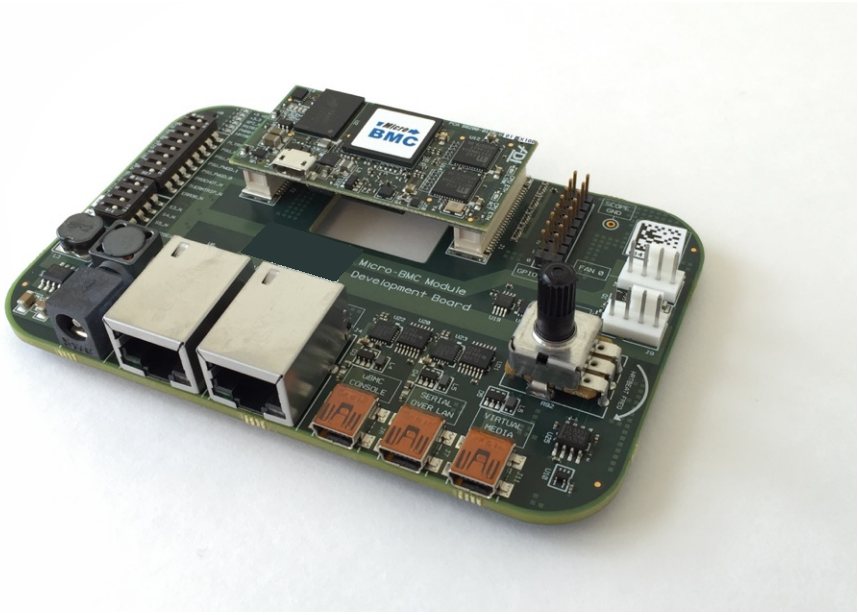
Micro-BMC (µBMC) Development Kit



User Manual

October 2015

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Revision History

Date	Revision	Remarks
10/6/15	R1.00	Initial version
10/14/15	R1.01	• Added photos
10/16/15	R1.02	• 1.1.1. Added micro-USB adapter and µBMC modules to kit contents.
10/16/15	R1.03	• 1.1.1, 2.1.2, 2.2.3, 3. Clarified that reference design modules are 256 MB (G00 version) and 512 MB (G01 version).
Date	R1.04	• Updated project logo

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1 CARRIER BOARD AND DEVELOPMENT KIT

1.1 Platform Description

1.1.1 Introduction

The micro-BMC (µBMC) is a miniature module that plugs into a connector site on server motherboards. It consists of a SoC and various I/O peripherals used to manage host CPU operations on the server motherboard.

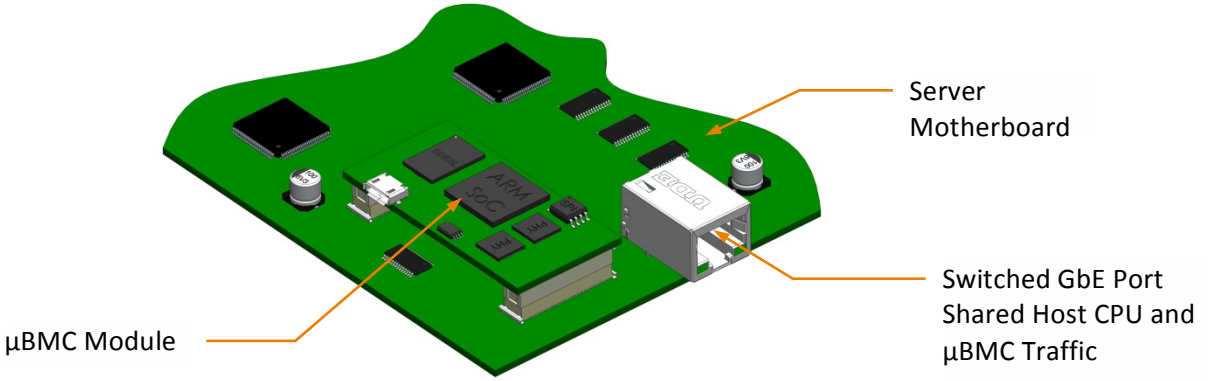


Figure 1 – Conceptual rendering of µBMC module mounted on server motherboard

The µBMC development kit is a tool used by firmware developers to debug their code with a simple desktop breakout of µBMC module I/O. This eliminates the need for an actual server motherboard during firmware development.

The kit consists of the following items:

- µBMC carrier board. ADI part number 80200-0129-G00.
- 120/240 VAC input +12 VDC output power adapter
- AC power cord
- Mini-USB cables (3)
- Micro-USB OTG male to USB-A host female adapter
- AM3352-based ARM µBMC module. 300 MHz CPU, 256 MB RAM.
- AM3352-based ARM µBMC module. 600 MHz CPU, 512 MB RAM.

Additional accessories and support plans can be ordered from ADI Engineering. See section 3 for optional accessories.

1.1.2 Feature summary

Feature	Description
LEDs	• Carrier board power • µBMC module discrete output signals
Host CPU heartbeat	• Knob sets heartbeat frequency to µBMC module
Voltage monitors	• Resistor dividers provide several DC voltages to µBMC module
Discrete inputs	• Discrete DIP switches set state to µBMC module • Host CPU health/status monitor signals • PSU powergood signals • ACPI signals
Host CPU boot flash	• SPI flash with simulated multiplexer
Fan control	• 2x +12 VDC 4-wire fan headers (PWM control, tach input)
Thermal sensors	• 1x LM75 discrete thermal sensor
Host CPU PECI monitor	• EEPROM for simulated PECI access via I2C bus
Serial over LAN	• USB UART brought out to mini-B connector (virtual COM port)
µBMC console	• USB UART brought out to mini-B connector (virtual COM port)
Virtual media	• USB brought out to mini-B connector (simulates connection to host CPU)
Ethernet	• Host CPU onboard: 1000base-T brought out to RJ-45 • Panel External: 1000base-T brought out to RJ-45
GPIO	• 8x GPIO pins brought out to header
Board form factor	• Desktop 2.9” x 4.6” (74 mm x 117 mm)
Power input	• 2.5mm barrel jack +12 VDC, 0.6 A max. • Does not include external +12 VDC fan current draw.

1.1.3 Block diagram

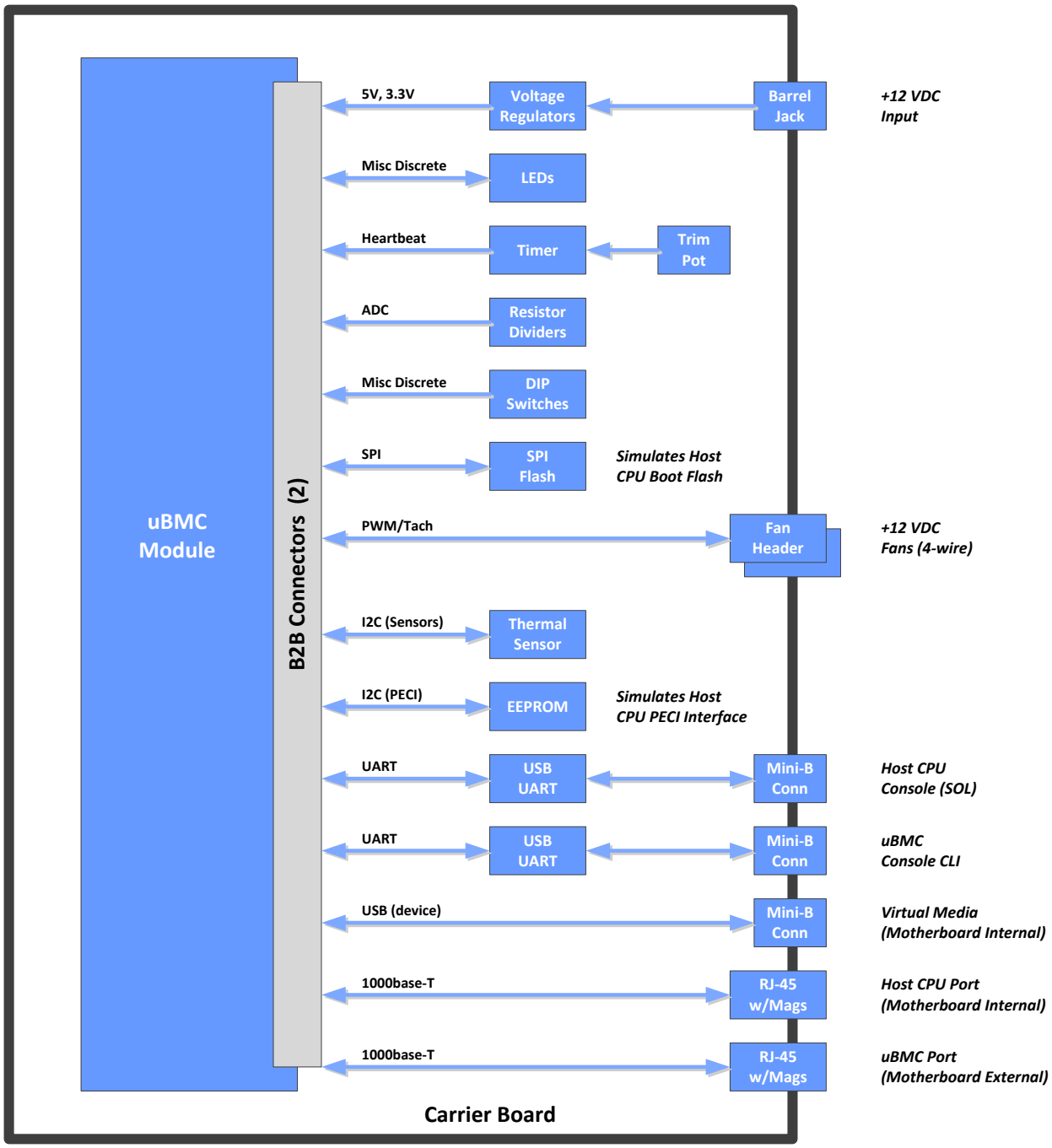


Figure 2 – Carrier board block diagram

1.2 User ports and features

1.2.1 Location of ports and features

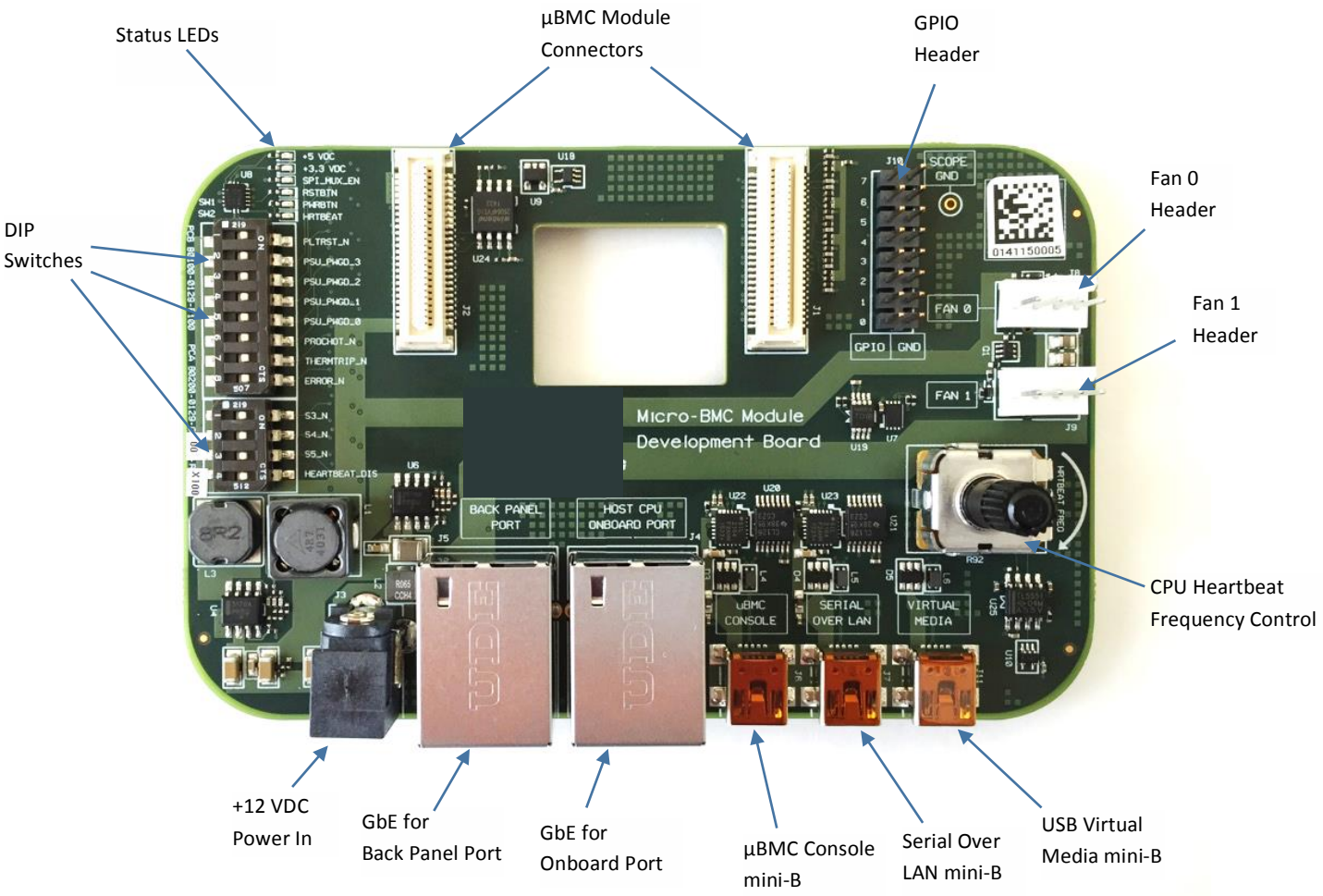


Figure 3 – Carrier board user ports and features locations

1.2.2 Status LEDs

The following status LEDs are provided:

LED	Color	Function
+5 VDC	GRN	Power good
+3.3 VDC	GRN	Power good
SPI_MUX_EN	GRN	On Mux set for µBMC module control of host CPU boot flash Off Mux set for host CPU control of boot flash
RSTBTN	GRN	On µBMC module has asserted host CPU reset button output low Off Host CPU reset button output deasserted high
PWRBTN	GRN	On µBMC module has asserted host CPU power button output low Off Host CPU power button output deasserted high
HRTBEAT	GRN	Flash Knob R92 sets host CPU heartbeat flash frequency to µBMC module

1.2.3 Host CPU heartbeat

Knob R92 is a potentiometer that sets the heartbeat frequency going to the µBMC module. Heartbeat period range is 70 ms to 1.46 ms. Turn the knob clockwise to increase the heartbeat frequency (decrease the period).

1.2.4 Voltage monitors

A total of 8 fixed resistor dividers set 8 different voltage inputs to the µBMC module voltage monitors. Voltages are assigned to the 8 µBMC module voltage monitor inputs as follows:

Voltage Monitor	Voltage Setting (VDC)
7	1.8
6	1.7
5	1.6
4	1.5
3	1.4
2	1.3
1	1.2
0	1.1

1.2.5 Discrete Inputs

A set of DIP switches are provided for simulating various motherboard status signals to the µBMC module, including:

- Host CPU health/status monitor signals
- PSU powergood signals
- ACPI signals

DIP switch assignments are listed in the following table.

Switch	Function	
PLTRST_N	On Off	Host CPU is in reset Host CPU normal operation
PSU_PWGD_3	On Off	Power supply unit 3 has failed Power supply unit 3 power output is good
PSU_PWGD_2	On Off	Power supply unit 2 has failed Power supply unit 2 power output is good
PSU_PWGD_1	On Off	Power supply unit 1 has failed Power supply unit 1 power output is good
PSU_PWGD_0	On Off	Power supply unit 0 has failed Power supply unit 0 power output is good
PROCHOT_N	On Off	Host CPU is approaching thermal limits and has begun throttling Host CPU normal operation
THERMTRIP_N	On Off	Host CPU has exceeded thermal limits and shut down Host CPU normal operation
ERROR_N	On Off	Host CPU operation error (MCERR, IERR, ERROR, etc.) Host CPU normal operation
S3_N	On Off	Host CPU is in S3 power state or below Host CPU is in S0 state
S4_N	On Off	Host CPU is in S4 power state or below Host CPU is in S0 or S3 state
S5_N	On Off	Host CPU is in S5 power state Host CPU is on S0, S3, or S4 power state
HEARTBEAT_DIS	On Off	Disable host CPU heartbeat Enable host CPU heartbeat

1.2.6 Host CPU boot flash

Some motherboards are designed with a multiplexer providing both host CPU and µBMC access to the host CPU boot flash. This allows the µBMC to perform host CPU boot flash firmware updates at the request of the Remote Administrator.

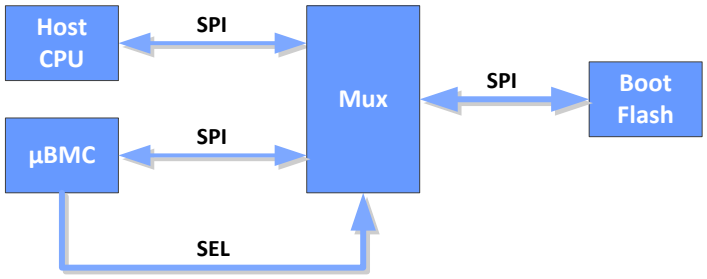
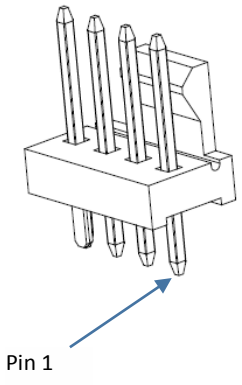


Figure 4 – Host CPU boot flash mux

The µBMC carrier board does not have an actual multiplexer, but does simulate a multiplexer by using the signal SPI_CPU_MUX_EN to gate the chip select to the SPI flash. The µBMC module drives SPI_CPU_MUX_EN high to control the host CPU boot flash and drives low to allow the host CPU access to the boot flash.

1.2.7 Fan control

Headers J8 and J9 can be connected to +12 VDC fans. The headers support 4-wire fans, but 2-wire and 3-wire fans will also work if only the necessary pins are connected. Header pinout as follows.



Pin	Function
1	+12 VDC
2	Tachometer
3	PWM
4	GND

Figure 5 – Fan header pinout

Mating connector is Molex 47054-1000 used with 22-30 AWG crimp terminal 0008500113 (reel) or 0008500114 (bag).

1.2.8 Thermal sensors

A standard LM75 type discrete temperature sensor is provided on the “Sensors” I2C bus at address 0x90.

1.2.9 Host CPU PECI monitor

The host CPU will typically have a SMBus slave port with internal registers which can be read by the µBMC module. This SMBus slave replaces the legacy PECI discrete signal. The register set includes current temperature of each CPU core, the core’s temperature rating, whether the core is operating normally or throttling performance, etc.

The µBMC carrier board does not have a true PECI SMBus slave. A simple EEPROM is provided at address 0xA0 to test SMBus access (“PECI” I2C bus).

1.2.10 Serial over LAN

The direct connection between µBMC module and host CPU console UART is simulated by bringing the µBMC UART connection out to a mini-USB-B connector J7 on the carrier board. A USB UART on the carrier board creates a virtual COM port on the developer’s computer which can be accessed with a terminal emulator like HyperTerminal, TeraTerm, etc. Connection speed is 115.2 Kbps.

1.2.11 µBMC console

The µBMC serial console port is brought out to a mini-USB-B connector J6 on the carrier board. A USB UART on the carrier board creates a virtual COM port on the developer’s computer which can be accessed with a terminal emulator like HyperTerminal, TeraTerm, etc. Connection speed is 1.0 Mbps.

1.2.12 Virtual media

The µBMC module provides a means for the Remote Administrator to boot the host CPU from a USB drive (thumbdrive, DVD drive, HDD, etc.) plugged into the Remote Administrator’s computer. The µBMC module does this by providing a USB device connection to the host CPU (host CPU is the USB host), identifying itself as a USB mass storage device type, and then mapping that USB device port to the LAN. Using this method, the Remote Administrator can remotely boot the host CPU from USB media for software installation, troubleshooting, etc. without requiring a local physical connection.

The µBMC virtual media USB port is brought out to a mini-USB-B connector J11 on the carrier board. This port can be used to remotely boot a laptop or desktop computer simulating a host CPU.

1.2.13 Ethernet

The µBMC module provides 2 switched GbE ports. These 2 ports are brought out to RJ-45 connectors. One RJ-45 connector J4 simulates the motherboard connection to the host CPU. The other RJ-45 connector J5 simulates the back panel external port.

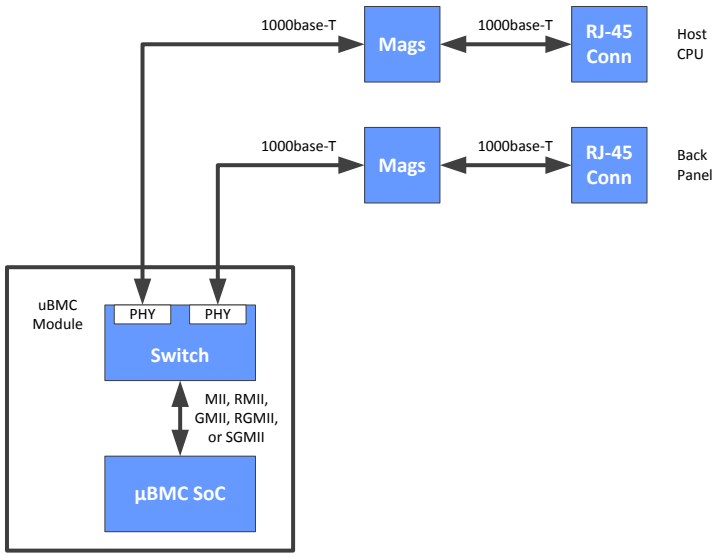


Figure 6 – Carrier board Ethernet topology

1.2.14 GPIO

The µBMC module provides 8 discrete GPIO signals. These 8x GPIO are brought out to pins on header J10. Each GPIO pin on the header has a corresponding GND pin for reference (if needed).

2 MICRO-BMC MODULE REFERENCE DESIGN

2.1 Platform description

2.1.1 Introduction

Silicom part number 80200-0128 is a µBMC module reference design based on the Texas Instruments AM3352 ARM CPU. All hardware and firmware features in the document "*micro-BMC open specification"* are implement ed. There are several variants of the module with different performance characteristics (CPU speed, memory d ensity, etc.). A list of orderable part numbers is provided in section 3.

2.1.2 Feature summary

See document "*micro-BMC open specification"* for a list of all features supported by pins on the board-to-board connectors.

Additional implementation-specific features are listed in the following table.

Feature	Description
CPU	• Variant G00: 300 MHz • Variant G01: 600 MHz
Memory	• Variant G00: 256 MB • Variant G01: 512 MB
Storage	• eMMC flash 4 GB
Boot flash	• SPI flash 8 MB
Status LEDs	• Module power • Module reset • Module boot flash activity • Host CPU (onboard) Ethernet port activity
User I/O	• Micro-USB-AB OTG connector for external boot storage (USB thumbdrive, etc.)

2.1.3 Block diagram

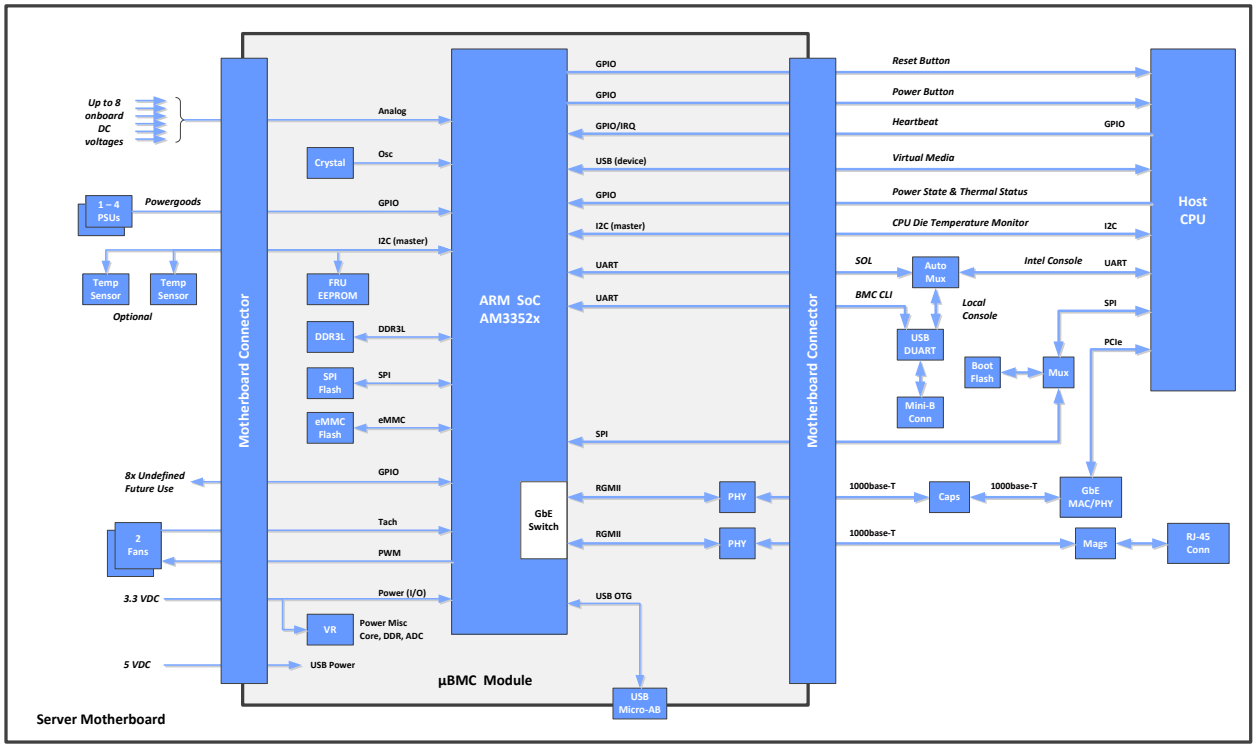


Figure 7 – Silicom µBMC module reference design block diagram

2.2 User ports and features

2.2.1 Location of ports and features

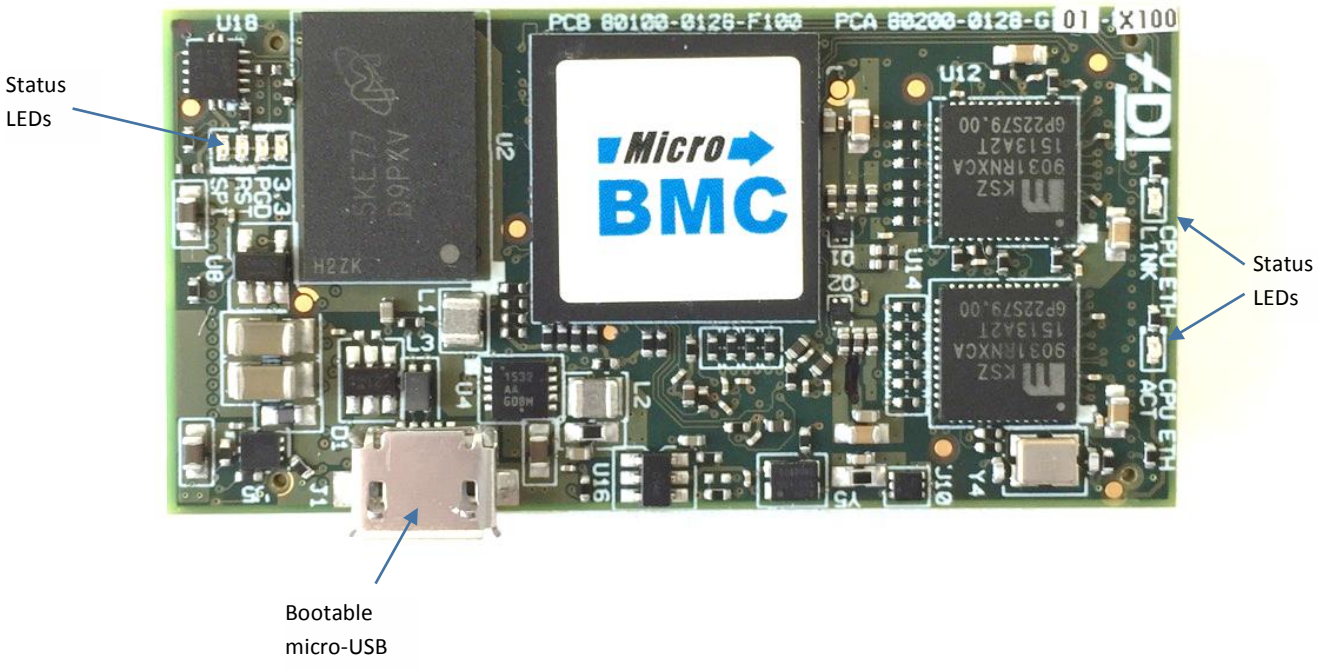


Figure 8 – Silicom µBMC module reference design user ports and features locations

2.2.2 CPU

The µBMC module reference design features a highly-integrated ARM CPU. There are several variant part numbers of the µBMC module with different CPU speeds supported as follows.

- Variant G00: Texas Instruments AM3352ZCZ30 (300 MHz)
- Variant G01: Texas Instruments AM3352ZCZ60 (600 MHz)

2.2.3 Memory

There are several variant part numbers of the µBMC module with different memory densities supported as follows.

- Variant G00: DDR3L-800, 16-bit, 256 MB. Reference Micron MT41K128M16JT-125.
- Variant G01: DDR3L-800, 16-bit, 512 MB. Reference Micron MT41K256M16HA-125:E.

2.2.4 Storage

The µBMC module reference design CPU has an integrated SD/MMC flash controller that is used with an onboard 4 GB eMMC flash device. The eMMC flash is a high-density Solid-State Disk (SSD) used for Operating System (OS) and data storage.

2.2.5 Boot flash

The µBMC module reference design CPU bootloader is contained in an onboard 8 MB SPI flash device.

2.2.6 Status LEDs

The following status LEDs are provided:

LED	Color	Function
3.3	GRN	+3.3 VDC power good
PGD	GRN	All power good (all onboard voltage regulators)
RST	GRN	On µBMC module is in reset Off Normal operation
CPU_ETH_LINK	GRN	On GbE link established with host CPU Off No link
CPU_ETH_ACT	GRN	Flash GbE activity between µBMC module and host CPU Off No activity

2.2.7 User I/O

A micro-USB-AB connector J1is provided on the side of the µBMC module for the USB 2.0 On The Go (OTG) port. This can be used with a micro-USB to USB-A host adapter to attach a USB thumbdrive, USB DVD drive, or other media (see accessories section 3). The µBMC module can be booted from the micro-USB port.

Figure 9 – Micro-USB to USB-A host adapter

2.3 Software considerations

2.3.1 Ethernet PHY configuration settings

The hardware connection between AM3352 CPU and the Micrel KSZ9031RNXCA Ethernet PHY is RGMII. One of the deficiencies in the RGMII specification is that the clock must be delayed relative to the data and control signals for the timing to work at the receiving end of the bus. Traditionally, this has been accomplished through long clock delay traces on the PCB layout. The µBMC module is physically too small to incorporate long clock delay traces.

Fortunately, the PHY has register setting options that can internally delay the clock, eliminating the need for external PCB trace delays. Specifically, the register settings must delay GTX_CLK relative to TXD[3:0] and TX_EN by 1.2 ns. The required register settings are listed in the following table.

Register	Address	Setting
RGMII control signal pad skew	MMD Address 2h, Register 4h	Bits 3:0 = 0x3
RGMII TX data pad skew	MMD Address 2h, Register 6h	Bits 15:0 = 0x3333
RGMII clock pad skew	MMD Address 2h, Register 8h	Bits 9:5 = 0x1F

2.3.2 PinMux Utility and Header Files

The Silicom µBMC module reference design ARM CPU pinout is defined in several header files generated by the T exas Instruments AM335x PinMux utility. These header files are available at the following software repository:

To Be Added

Many of the CPU pins can have multiple functions, which are routed through internal multiplexers. The header files define the multiplexer setting for each pin to ensure that the correct function for the reference design is mapped to that pin.

2.3.3 ARM CPU Pin mapping

The AM3352 CPU in the ZCZ package has the pinout described in the following table.

Notes:

- NC denotes no connect (floating on board)
- N/A (strapping pin) denotes a pin that is connected to external pullup/pulldown for boot strapping options, but is not connected to any signal.
- All of the pullups/pulldowns and mux settings are in the supplied PinMux header files (section 2.3.2).

Pin	Pin Name	PCB Signal	I/O	Internal PU/PD	Function
U7	GPMC_AD0	EMMC_D0	I/O		eMMC flash SSD data
V7	GPMC_AD1	EMMC_D1	I/O		eMMC flash SSD data
R8	GPMC_AD2	EMMC_D2	I/O		eMMC flash SSD data
T8	GPMC_AD3	EMMC_D3	I/O		eMMC flash SSD data
U8	GPMC_AD4	EMMC_D4	I/O		eMMC flash SSD data
V8	GPMC_AD5	EMMC_D5	I/O		eMMC flash SSD data
R9	GPMC_AD6	EMMC_D6	I/O		eMMC flash SSD data
T9	GPMC_AD7	EMMC_D7	I/O		eMMC flash SSD data
U10	GPMC_AD8	NC			No connect
T10	GPMC_AD9	NC			No connect
T11	GPMC_AD10	NC			No connect
U12	GPMC_AD11	NC			No connect
T12	GPMC_AD12	GPIO3	I/O		User GPIO (undefined)
R12	GPMC_AD13	NC			No connect
V13	GPMC_AD14	NC			No connect
U13	GPMC_AD15	NC			No connect
R13	GPMC_A0	RGMII_2_TX_EN	O	PD	RGMII port 2 transmit enable
V14	GPMC_A1	RGMII_2_RX_DV	I		RGMII port 2 receive data valid
U14	GPMC_A2	RGMII_2_TXD3	O	PD	RGMII port 2 transmit data
T14	GPMC_A3	RGMII_2_TXD2	O	PD	RGMII port 2 transmit data
R14	GPMC_A4	RGMII_2_TXD1	O	PD	RGMII port 2 transmit data
V15	GPMC_A5	RGMII_2_TXD0	O	PD	RGMII port 2 transmit data
U15	GPMC_A6	RGMII_2_TX_CLK	O	PD	RGMII port 2 transmit clock

Pin	Pin Name	PCB Signal	I/O	Internal PU/PD	Function
T15	GPMC_A7	RGMII_2_RX_CLK	I		RGMII port 2 receive clock
V16	GPMC_A8	RGMII_2_RXD3	I		RGMII port 2 receive data
U16	GPMC_A9	RGMII_2_RXD2	I		RGMII port 2 receive data
T16	GPMC_A10	RGMII_2_RXD1	I		RGMII port 2 receive data
V17	GPMC_A11	RGMII_2_RXD0	I		RGMII port 2 receive data
T17	GPMC_WAIT0	CPU_THERMTRIP_N	I		Host CPU thermal trip (overtemp)
U17	GPMC_WPN	GPIO2	I/O		User GPIO (undefined)
U18	GPMC_BEN1	GPIO5	I/O		User GPIO (undefined)
V6	GPMC_CSN0	USB_OC_N	I		Micro-USB port overcurrent
U9	GPMC_CSN1	EMMC_CLK	O		eMMC flash SSD clock
V9	GPMC_CSN2	EMMC_CMD	I/O		eMMC flash SSD command
T13	GPMC_CSN3	NC			No connect
V12	GPMC_CLK	NC			No connect
R7	GPMC_ADVN_ALE	CPU_SLP_S3_N	I		Host CPU ACPI state S3 or below
T7	GPMC_OEN_REN	CPU_ERROR_N	I		Host CPU error
U6	GPMC_WEN	GPIO0	I/O		User GPIO (undefined)
T6	GPMC_BEN0_CLE	CPU_SLP_S5_N	I		Host CPU ACPI state S5
R1	LCD_DATA0	FAN_PWM1	O		Fan 1 PWM speed control
R2	LCD_DATA1	N/A (strapping pin)			
R3	LCD_DATA2	N/A (strapping pin)			
R4	LCD_DATA3	N/A (strapping pin)			
T1	LCD_DATA4	N/A (strapping pin)			
T2	LCD_DATA5	N/A (strapping pin)			
T3	LCD_DATA6	N/A (strapping pin)			
T4	LCD_DATA7	N/A (strapping pin)			
U1	LCD_DATA8	N/A (strapping pin)			
U2	LCD_DATA9	N/A (strapping pin)			
U3	LCD_DATA10	FAN_PWM0	O		Fan 0 PWM speed control
U4	LCD_DATA11	N/A (strapping pin)			
V2	LCD_DATA12	N/A (strapping pin)			
V3	LCD_DATA13	N/A (strapping pin)			
V4	LCD_DATA14	N/A (strapping pin)			
T5	LCD_DATA15	N/A (strapping pin)			

Pin	Pin Name	PCB Signal	I/O	Internal PU/PD	Function
U5	LCD_VSYNC	CPU_PLTRST_N	I		Host CPU platform reset
R5	LCD_HSYNC	CPU_SLP_S4_N	I		Host CPU ACPI state S4 or below
V5	LCD_PCLK	TESTPOINT_SPARE	I/O		Spare GPIO pin for debug use
R6	LCD_AC_BIAS_EN	GPIO1	I/O		User GPIO (undefined)
F17	MMC0_DAT3	GPIO4	I/O		User GPIO (undefined)
F18	MMC0_DAT2	CPU_PWRBTN_N	O		Host CPU power button control
G15	MMC0_DAT1	CPU_PROCHOT_N	I		Host CPU nearing overtemp and throttling
G16	MMC0_DAT0	NC			No connect
G17	MMC0_CLK	UART_SOL_RXD	I	PU	Host CPU serial over LAN receive
G18	MMC0_CMD	UART_SOL_TXD	O		Host CPU serial over LAN transmit
H16	MII1_COL	SPI_CPU_SCK	O		Host CPU boot flash SPI clock
H17	MII1_CRS	SPI_CPU_MISO	I		Host CPU boot flash SPI data in
J15	MII1_RX_ER	SPI_CPU_MOSI	O		Host CPU boot flash SPI data out
J16	MII1_TX_EN	RGMII_1_TX_EN	O	PD	RGMII port 1 transmit enable
J17	MII1_RX_DV	RGMII_1_RX_DV	I		RGMII port 1 receive data valid
J18	MII1_TXD3	RGMII_1_TXD3	O	PD	RGMII port 1 transmit data
K15	MII1_TXD2	RGMII_1_TXD2	O	PD	RGMII port 1 transmit data
K16	MII1_TXD1	RGMII_1_TXD1	O	PD	RGMII port 1 transmit data
K17	MII1_TXD0	RGMII_1_TXD0	O	PD	RGMII port 1 transmit data
K18	MII1_TX_CLK	RGMII_1_TX_CLK	O	PD	RGMII port 1 transmit clock
L18	MII1_RX_CLK	RGMII_1_RX_CLK	I		RGMII port 1 receive clock
L17	MII1_RXD3	RGMII_1_RXD3	I		RGMII port 1 receive data
L16	MII1_RXD2	RGMII_1_RXD2	I		RGMII port 1 receive data
L15	MII1_RXD1	RGMII_1_RXD1	I		RGMII port 1 receive data
M16	MII1_RXD0	RGMII_1_RXD0	I		RGMII port 1 receive data
H18	RMII1_REF_CLK	SPI_CPU_CS_N	O		Host CPU boot flash SPI chip select
M17	MDIO	MDIO	I/O		PHY management data
M18	MDC	MDC	O	PU	PHY management clock
A17	SPI0_SCLK	SPI_BOOT_CLK	O		AM3352 boot flash SPI clock
B17	SPI0_D0	SPI_BOOT_MISO	I		AM3352 boot flash SPI data in
B16	SPI0_D1	SPI_BOOT_MOSI	O		AM3352 boot flash SPI data out
A16	SPI0_CS0	SPI_BOOT_CS_N	O		AM3352 boot flash SPI chip select
C15	SPI0_CS1	FAN_TACH0	I		Fan 0 tachometer (speed) input

Pin	Pin Name	PCB Signal	I/O	Internal PU/PD	Function
C18	ECAP0_IN_PWM0_OUT	CPU_HEARTBEAT_N	I		Host CPU user application heartbeat
E18	UART0_CTSN	I2C_PECI_SDA	I/O		Host CPU PECI thermal monitor data
E17	UART0_RTSN	I2C_PECI_SCL	O		Host CPU PECI thermal monitor clock
E15	UART0_RXD	UART_CLI_RXD	I		AM3352 serial console receive
E16	UART0_TXD	UART_CLI_TXD	O		AM3352 serial console transmit
D18	UART1_CTSN	NC			No connect
D17	UART1_RTSN	NC			No connect
D16	UART1_RXD	EMMC_WP	I	PD	eMMC flash SSD write protect
D15	UART1_TXD	CPU_RSTBTN_N	O		Host CPU reset button control
C17	I2C0_SDA	I2C_SENSORS_SDA	I/O		EEPROM and thermal sensors I2C data
C16	I2C0_SCL	I2C_SENSORS_SCL	O		EEPROM and thermal sensors I2C clock
A13	MCASP0_ACLKX	PSU_PWRGD1	I		Power supply unit 1 power good
B13	MCASP0_FSX	EMMC_CD	I	PU	eMMC flash SSD card detect
D12	MCASP0_AXR0	SPI_CPU_MUX_EN	O		Host CPU boot flash multiplexer control
C12	MCASP0_AHCLKR	FAN_TACH_1	I	PD	Fan 1 tachometer (speed) input
B12	MCASP0_ACLKR	PSU_PWRGD0	I		Power supply unit 0 power good
C13	MCASP0_FSR	GPIO6	I/O		User GPIO (undefined)
D13	MCASP0_AXR1	NC			No connect
A14	MCASP0_AHCLKX	PSU_PWRGD2	I		Power supply unit 2 power good
A15	XDMA_EVENT_INTR0	PSU_PWRGD3	I		Power supply unit 3 power good
D14	XDMA_EVENT_INTR1	GPIO7	I/O		User GPIO (undefined)

3 OPTIONAL ACCESSORIES AND SUPPORT PACKAGES

The following optional accessories and support packages can be ordered from Silicom Ltd.

Description	ADI Part Number
AM3352-based ARM µBMC module. 300 MHz CPU, 256 MB RAM.	80200-0128-G00
AM3352-based ARM µBMC module. 600 MHz CPU, 512 MB RAM.	80200-0128-G01
Micro-USB OTG male to USB-A host female adapter, 5”	28150-0034

Corporate sales: www.silicom-usa.com
Phone: (972) 9-7644555

4 ABOUT SILICOM LTD.

4.1 Company information

Silicom Ltd. is an industry-leading provider of high-performance networking and data infrastructure solutions. Designed primarily to improve performance and efficiency in Cloud and Data Center environments, Silicom's solutions increase throughput, decrease latency and boost the performance of servers and networking appliances, the infrastructure backbone that enables advanced Cloud architectures and leading technologies like NFV, SD-WAN and Cyber Security. Our innovative solutions for high-density networking, high-speed fabric switching, offloading and acceleration, which utilize a range of cutting-edge silicon technologies as well as FPGA-based solutions, are ideal for scaling-up and scaling-out cloud infrastructures.

Silicom products are used by major Cloud players, service providers, telcos and OEMs as components of their infrastructure offerings, including both add-on adapters in the Data Center and stand-alone virtualized/universal CPE devices at the edge.

Silicom's long-term, trusted relationships with more than 150 customers throughout the world, its more than 400 active Design Wins and more than 300 product SKUs have made Silicom a "go-to" connectivity/performance partner of choice for technology leaders around the globe.

4.2 Contacts

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