Silicom Connectivity Solutions

PE3100G2DQIR8

Dual port Fiber 100 Gigabit Ethernet PCI Express Content Director Server Adapter

Product Description

Silicom's 100/40 Gigabit Ethernet PCI Express content aware director server adapters is designed for servers and high-end appliances. The Silicom content aware director server adapter is designed with an on board smart routing architecture that enables packets to be redirected or dropped based on defined rules.

The Silicom's 100/40 Gigabit Ethernet content aware packet director reduces host system process since only packets that are defined to be targeted to the host systems are routed to the host; other packets can be routed to the other port or can be dropped by the content aware hardware routing architecture.

The Silicom's 100/40 Gigabit Ethernet content aware packet director is targeted to network applications that needs to process, monitor or bypass packets based on defined rules. The adapter supports three main modes of operation: Content Aware Bypass, Content Aware TAP and content Aware filtering NIC.

Content Aware Bypass

Silicom's 100/40 Gigabit Ethernet content aware director provides intelligent packet redirection capability where rules specify which packets are directed to the host system and which packets are directed to the other port (Bypass).

Content Aware TAP

Silicom's 100/40 Gigabit Ethernet content aware director provides intelligent packet redirection capability where all packets are directed to the other port (Bypassed) and rules specify which packets are copied to the host system (TAP).

Content Aware Filtering NIC

Silicom's 100/40 Gigabit Ethernet content aware provides intelligent packet redirection capability where rules specify which packets are directed to the host or dropped.

The Silicom 100/40 Gigabit Ethernet PCI Express content director server adapter is based on Intel FM10840 Ethernet controller and a L3 switch router. The Silicom's 40 Gigabit Ethernet PCI Express adapter is based on standard L2 driver and with the content director engine reduces CPU host system processing.

The Silicom 100/40 Gigabit Ethernet PCI Express content aware server adapter offers simple integration into any PCI Express X16 to 100Gigabit Network.

Key Features

Content Aware Director:

- Provides intelligent packet redirection capability where rules specify which packets are directed to the host system and which packets are directed to the other port (Bypass).
- Provides intelligent packet redirection capability where all packets are directed to the other port (Bypassed) and rules that specify which packets are copied to the host system (TAP).
- Provides intelligent packet filtering / drop capability where rules specify which packets are directed to the host or dropped.
- Provides redirection rules that can be defined using source IP/ destination IP / Source Port / Destination Port / VLAN tuples.
- Redirection and packet filtering / drop are performed by the hardware itself in wire speed and do not require any software and CPU host system power processing.
- Intelligent redirect mechanism is controllable via software.
- Intelligent routing mechanism is controllable via software.
- Support 2x100G / QSFP28 ports.
- 100G QSFP28 Ports support 100GBase-SR4 and 100GBase-LR4.
- 40G QSFP28 Ports support 40GBase-SR4 and 40GBase-LR4.

Common Key features:

- **Host Interface:**
- PCI Express X16 lane
- Support PCI Express Base Specification Revision 3.0, 8GT/s, 5GT/s or 2.5GT/s

Intel FM10840 Features:

- Single-element 4MB shared memory
- L2/L3/L4/OpenFlow forwarding & ACLs
- Stateless load balancing to CPUs
- Datacenter Bridging (lossless Ethernet)
- 32K 40-bit TCAM entries
- 16K MAC & NextHop tables
- Up to 300Gbps High-bandwidth CPU interface
- 2x 50Gbps 8-lane PCIe interfaces
- Up to 8 25G/10G/2.5G/1G ports
- Up to 2 40G (4 x 10G)

- Up to 2 100G (4 x 25G)
- 300ns network latency (100GbE)
- 1000nS host-network latency

LAN Features:

- 256 queues per PCIe x16 interface
- SR-IOV (64 VFs per PCIe x16 interface)
- IP/TCP/UDP checksum
- Receive side scaling (RSS)
- TCP segmentation offload (TSO/LSO)
- LEDs indicator for link/Activity.

Technical Specifications

–QX4: QSFP+ 40Gigabit Ethernet Technical Specifications Adapters:	
QSFP+ (Quad Small Form-factor Pluggable) supports:	XLPPI interfaces supports 40GBase-R PCS and 40 Gigabit PMA in order to connect with QSFP+ to 40GBase-SR4 / 40GBase-LR4
IEEE Standard / Network topology: with 40GBase-SR4 QSFP+	Fiber 40Gigabit Ethernet, 40GBASE-SR4 (850nm LAN PHY).
IEEE Standard / Network topology: with 40GBase-LR4 QSFP+	Fiber 40Gigabit Ethernet, 40GBASE-LR4 (1310nm LAN PHY)
-ZS4: Fiber 100GBASE-SR4 Ethernet Technical Specifications:	
IEEE Standard / Network topology:	Fiber Gigabit Ethernet, 100GBase-SR4 (850nM)
Data Transfer Rate:	103.125GBd
Cables and Operating distance: Up to:	Multimode fiber: 62.5um, (OM4) 100m
Optical Output Power:	Typical: TBD dBm Minimum: TBD dB * being defined by IEEE 802.3bm

Optical Receive Sensitivity:	Typical: TBD dBm Maximum: TBD dBm * being defined by IEEE 802.3bm
– ZL4: Fiber 100GBASE-LR4 Ethernet Technical Specifications:	
IEEE Standard / Network topology:	Fiber 100Gigabit Ethernet, 100GBASE-LR4 (1310nM)
Data Transfer Rate:	103.1GBd
Cables and Operating distance: Up to:	Single-Mode: 10km
Optical Output Power:	Typical: TBD dBm Minimum: -4.3 dBm
Optical Receive Sensitivity:	Typical: TBD dBm Maximum: -10.6 dBm
– QS41: Fiber 40GBASE-SR4 Ethernet Technical Specifications:	
IEEE Standard / Network topology:	Fiber 40Gigabit Ethernet, 40GBASE-SR4 (840 to 860 nm LAN PHY). IEEE 802.3ba
Data Transfer Rate:	10.5 GBd per lane
Cables and Operating distance:	50um, (OM3) 1500 MHz*Km, 0.5 to 100 m 50um, (OM4) 3500 MHz*Km, 0.5 to 150 m
Output Transmit Power:	Maximum: 2.4 dBm per lane Minimum: -7.6 dBm per lane
Optical Receive Sensitivity:	Minimum: -5.4 dBm
Maximum Input Power:	Maximum: 2.4 dBm
– QS43: Fiber 40GBASE-SR4 Ethernet Technical Specifications:	
IEEE Standard / Network topology:	Fiber 40Gigabit Ethernet, 40GBASE-SR4 (840 to 860 nm LAN PHY). IEEE 802.3ba

Data Transfer Rate:	10.5 GBd per lane
Cables and Operating distance:	50um, (OM3) 1500 MHz*Km, 0.5 to 300 m 50um, (OM4) 3500 MHz*Km, 0.5 to 400 m
Output Transmit Power:	Maximum: 0.5 dBm per lane Minimum: -7.5 dBm per lane
Optical Receive Sensitivity:	Minimum -7.5dBm
Maximum Input Power:	Maximum: 2.4 dBm
– QL4: Fiber 40GBASE-LR4 Ethernet Technical Specifications:	
IEEE Standard / Network topology:	Fiber 40Gigabit Ethernet, 40GBASE-LR4 (1264.5nm – 1277.5nm ; 1284.5nm – 1297.5nm ; 1304.5nm – 1317.5nm ; 1324.5nm – 1337.5nm LAN PHY). IEEE 802.3ba
Data Transfer Rate:	10.3125 GBd per lane
Cables and Operating distance:	SMF-28, 10Km
Output Transmit Power:	Maximum: 2.3 dBm per lane Minimum: -7.0dBm per lane
Optical Receive Sensitivity:	Maximum: -9.6 dBm
Maximum Input Power:	Maximum: 2.3 dBm
Operating Systems Support:	
Operating system support:	Linux
General Technical Specifications:	
Interface Standard:	PCI-Express Base Specification Revision 3.0(8 GTs)
Board Size:	Standard height long add-in card 203.2mm X 111.15mm (8”X 4.376”)
PCI Express Card Type:	X16 Lane

PCI Express Voltage:	+12V ± 8%
External Voltage from external PW jack:	+12V ± 8%
PCI Connector:	Gold Finger: X16 Lane
Controller:	Intel FM10840
Holder:	Metal Bracket
Operating Humidity:	0%–90%, non-condensing
Operating Temperature:	0°C – 40°C (32°F – 104°F), Air flow requirement 200FLM
Storage:	-40°C–65°C (-40°F–149°F)
Regulation:	Card shall meet CE, FCC Class B, ROHS requirements.
MTBF*:	* The prediction was performed for 40°C Ambient temperature, GB Environmental condition. The reliability prediction was performed in accordance with Telcordia SR-332.
-LEDs/ Connectors Specifications:	
LEDs:	Four LEDs per port (1) Link/Act 100/25/10Gbps LED: Turns on – link, Blink – ACT 100Gbps(Yellow) 25Gbps(Orange) 10Gbps(Blue) (1) Link/Act 40/25/10Gbps LED: Turns on – link, Blink – ACT 40Gbps(Yellow) 25Gbps(Orange) 10Gbps(Blue) (2) Link/Act 25/10Gbps LEDs: Turns on – link, Blink – ACT 25Gbps(Orange) 10Gbps(Blue)
LEDs location:	LEDs are located on the PCB, visible by light quide in the metal bracket.
Connector:	(2) MPO/LC

Functional Description

Director Director – Content Aware Bypass

Silicom's 100 Gigabit Ethernet content aware director Provides intelligent packet redirection capability where rules specify which packets are directed to the host system and which packets are directed to the other port (Bypass).

Figure 1: Content Aware Bypass Functional Block Diagram

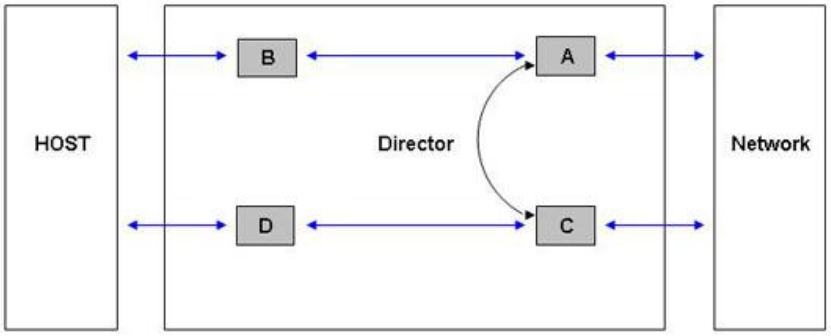

Figure 1 Content Aware Bypass Functional Block Diagram

Figure 1 illustrates functional block diagram of content aware Bypass:

Packets received in port A and meet rule are directed to port B, other packets are directed to port C (Bypass).

Packets received in port C and meet rule are directed to port D, other packets are directed to port A (Bypass).

Director – Content Aware TAP

Silicom's 100 Gigabit Ethernet content aware director Provides intelligent packet redirection capability where all packets are directed to the other port (Bypassed) and rules specify which packets are copied to the host system (TAP).

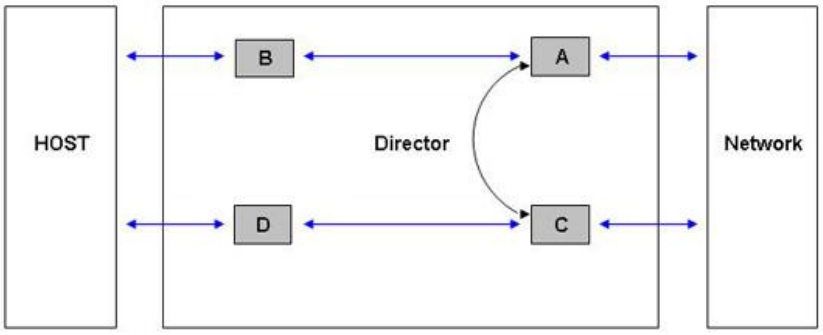

Figure 2: Content Aware TAP Functional Block Diagram

Figure 2 illustrates functional block diagram of content aware TAP:

Packets received in port A and meet rule are directed to ports B and C (TAP), other packets are directed to port C (Bypass).

Packets received in port C and meet rule are directed to ports D and A (TAP), other packets are directed to port A (Bypass).

Director – Content Filtering NIC

Silicom's 100 Gigabit Ethernet content aware provides intelligent packet redirection capability where rules specify which packets are directed to the host or dropped.

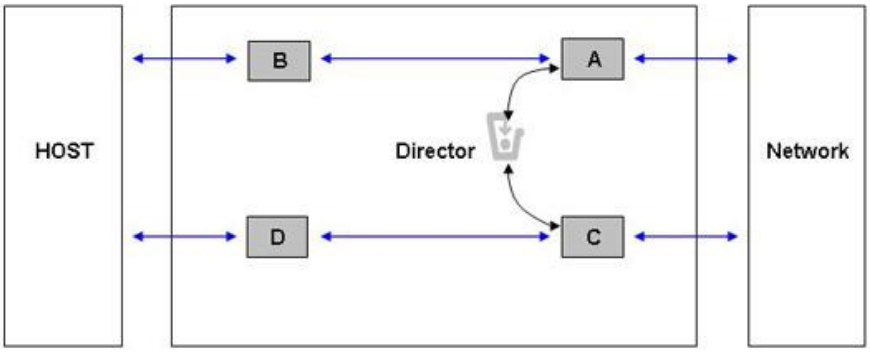

Figure 3: Content Aware Filtering NIC Functional Block Diagram

Figure 3 illustrates functional block diagram of content aware TAP:
Packets received in port A and meet rule, direct to port B. Packets received in port A and do not meet rule are dropped.
Packets received in port C and meet rule, direct to port D. Packets received in port C and do not meet rule are Dropt.

Director: Rules Classification and capabilities

The Redirector supports the following capabilities:

Maximum total number of rules is 16K.

Each of the 16K rules can be defined to any port the on board multi-layer switch.

Each rule refers to incoming packet

Rules are executed per order. First rule that matches will be executed

Rules can be added and removed on the fly.

Each rule can include one or more classification fields. A rule match will be when all fields defined are match.

Each field can have a bit masking to check part of the classification field.

Per port statistics can be read, like packets count, errors, VLAN, and more.

Rules and action are done in wire speed at any packet size.

Rules classification fields

Rules classification is done based on the first 128 bytes of the packets. The following list provides rules classification fields.

MAC address, source & destination

IPv4 – source & destination IP

IPv6 – source & destination IP

L4 Port – source & destination port

Ethernet Protocol – ethertype

IP Protocol num.

VLAN ID tagging

User defined fields

DSCP – match the different services code point – the six most significant bits of the Type of Service octet (IPv4) or Traffic Class octet (IPv6).*

IPv6 Flow Label*

IP length*

ISL Frame Type*

ISL USER*

Source & destination port range*

VLAN priority*

VLAN tag type*

TCP flags*

TOS – match Type of Service octet (IPv4) or Traffic Class octet (IPv6)*

TTL field in a IPv4 header or Hop Limit in a IPv6 header*

*Future SW supports.

Execution per rule

The following Executions per rule are supported:

Drop – when a rule matches the packet will be dropped
Redirect – when a rule matches redirect the packet to the defined destination port
Mirror – when a rule matches copy packet also to a defined destination port

Director Advanced Features:
Director Advanced features*

Port trunking between the Intel port to the Intel port connected to it for load balancing between the different Intel ports

Port trunking between the different External Intel port to the external switch connected to it for load balancing between the different external ports.

Session balancing with L3/L4 hashing or other mechanism

ISL (Inter Switch Link) Tagging per port can be added to the packets per configuration

ISL Tagging can be removed and can be forward to specific port per the ISL index.

Quality of Service support with the following features:

Priority levels: 16 internal “switch” priorities, 8 or 16 VLAN priorities (optional use of CFI bit as an extra VLAN priority bit)

Arbitrary mapping of ingress VLAN priority to an internal VLAN priority

Arbitrary mapping of an internal VLAN priority to egress VLAN priority

Arbitrary mapping of internal VLAN priority to switch priority

Arbitrary mapping of DSCP to switch priority, configurable priority source selection.

Scheduler: 8 traffic classes, arbitrary mapping of switch priorities to traffic class, deficit weighted round-robin or strict priority.

Notification: Two congestion notifications can be supported;

Virtual output queue congestion notification (VCN) and Intel proprietary backward congestion notification (FCN).

Open Flow support (consistent with OpenFlow protocol standard)

sFlow support

User defined Packet transmission with two optional modes: 1. Simple mode – transmit on specific port. 2. Switched mode – where switch determines destination port/ports, or with specific information such as whether or not egress processing rules should be applied.

Storm Control Management – Switch can support a variety storm controller. Each storm controller can be programmable to define rat, condition (like unicast ICMP frames whose TTL is at most 1), frame type (can be OR'ed), ingress & egress port ports. Actions: do nothing, drops frames to port (according to filter)

*Future SW supports.

Order Information

Thermal Sensing

Temp Sensor	Address	Thermal Diode and placement
ADT7475	0101_110x	D1 (Reg 0x25): Internal Diode on RRC (Tj) Local (Reg 0x26): PS , back edge (Tj) D2 (Reg 0x27): Internal Diode on PLX (Tj)

P/N	Description	Notes
PE3100G2DQIR8-ZS4	Dual port Fiber (SR4) 100 Gigabit Ethernet PCI Express Content Director Server Adapter	RoHS Compliant, X16 Gen 3, based on Intel FM10840
PE3100G2DQIR8-ZL4	Dual port Fiber (LR4) 100 Gigabit Ethernet PCI Express Content Director Server Adapter	RoHS Compliant, X16 Gen 3, based on Intel FM10840
PE3100G2DQIR8-QS41	Dual port Fiber (SR4) 40 Gigabit Ethernet PCI Express Content Director Server Adapter	RoHS Compliant, X16 Gen 3, based on Intel FM10840, on board support for Fiber SR4 up to length 100m on OM3 MMF

PE3100G2DQIR8-QS43	Dual port Fiber (SR4) 40 Gigabit Ethernet PCI Express Content Director Server Adapter	RoHS Compliant, X16 Gen 3, based on Intel FM10840, on board support for Fiber SR4 300m on OM3 MMF
PE3100G2DQIR8-QL4	Dual port Fiber (LR4) 40 Gigabit Ethernet PCI Express Content Director Server Adapter	RoHS Compliant, X16 Gen 3, based on Intel FM10840, on board support for Fiber LR4
PE3100G2DQIR8-Qx4	Dual port Fiber (LR4) 40 Gigabit Ethernet PCI Express Content Director Server Adapter	RoHS Compliant, X16 Gen 3, based on Intel FM10840, on board support for QSFP+

1V3