OE2G2I35

Dual Port Copper Gigabit Ethernet OCP Mezzanine Adapter Intel® I350BT2 Based

Product Description

Silicom's Gigabit Ethernet Open Compute Project (OCP) mezzanine adapter is designed for use with Open Compute Project (OCP) Intel V2.0 Mother boards.

The Silicom's Gigabit Ethernet OCP mezzanine dual Gigabit Ethernet connectivity to the OCP Server node. The Silicom Copper Gigabit Ethernet OCP mezzanine adapter is based on Intel I350BT2 Ethernet controller with two fully integrated Gigabit Ethernet Media Access Control (MAC) and PCI Express x4 Genereation 2.

The Silicom Copper Gigabit Ethernet OCP mezzanine adapter implement a type C NC-SI interface (single package, common bus buffers and shared RX queue).

Silicom's Copper Gigabit Ethernet OCP Mezzanine adapters is the ideal solution for implementing multiple network segments, mission-critical high-powered networking applications and environments within high performance OCP servers.

Key Features

Host Interface:

- Supports Open Compute Project Mezzanine Specification V0.3 form factor
- Supports FCI 61083-124402LT or equivalent mounted on the mezzanine adapter
- PCI Express X4 lanes, 5GT/s
- NC-SI for Manageability connection to BMC

Copper Gigabit Ethernet 1000Base-T :

- Independently copper Gigabit Ethernet channels support two Gigabit Ethernet (1000Base-T), Fast Ethernet (100Base-Tx) and Ethernet (10Base-T)
- Triple speed 1000Mbps (1000Base-T), 100 Mbps (100Base-Tx) and 10 Mbps (100Base-T) operation
- Nway auto negotiation automatic sensing and switching between 1Gbps full duplex and 100 / 10 Mbps operations Simplex or Full Duplex
- RJ-45 female connectors

Performance Features:

- 8 Transmit and 8 Receive queues per port
- Up to8 queues of Receive Side Scaling (RSS) minimize CPU utilization across multiple processor systems
- Support PCI-SIG Single-Root I/O virtualization Rev 1.1
- Support for up to 8 virtual function (VFs)
- Partial replication of PCI Configuration space
- Support for 8 pools (single queue) of virtual machine Device Queues (VMDq) per port
- Support Direct Cache Access (DCA)
- Support Intel I/O Acceleration Technology v3.0
- TSO interleaving for reduced latency
- Minimized device I/O interrupts using MSI and MSI-X
- UDP, TCP and IP checksum offload
- UDP and TCP transmit segmentation offload (TSO). machine
- SCTP receive and transmit checksum offload
- Packet interrupt coalescing timers (packet timers) and absolute-delay interrupt timers for both transmit and receive operation
- EEE (IEEE 802.3az) for reduced power consumption during low link utilization periods

Common Key features:

- Support PCI Express Base Specification 2.1 (5 GTs)
- High performance, reliability, and low power use in Intel I350 Dual integrated MAC + PHY and SERDES chip Controllers
- Ultra deep, packet buffer per channel lowers CPU utilization
- Hardware acceleration that can offload tasks from the host processor. The Controllers can offload TCP/UDP/IP checksum calculations and TCP segmentation
- Server class reliability, availability and performance features:
- Link Aggregation and Load Balancing
- Priority queuing –802.1p layer 2 priority encoding
- Virtual LANs –802.1q VLAN tagging
- Jumbo Frame (9.5KB)
- 802.x flow control
- Multicast/ broadcast Packet replication
- Supports Vital Product Data (VPD)
- LEDs indicators for link/Activity/Speed status

LAN Features:

- IEEE 802.x flow control support
- IEEE 802.1q VLAN tagging support
- IEEE 802.1p layer 2 priority encoding
- Jumbo Frame (up to 15.5KB)
- Link Aggregation and Load Balancing
- RFC2819 RMON MIB statistics
- TCP Segmentation Offload Up to 256KB
- Ipv6 Support for IP/TCP Receive Checksum Offload
- LEDs indicator for link/Activity

Technical Specifications

Operating Systems Support	
Operating system support:	Windows Linux FreeBSD VMware
General Technical Specifications	
Interface Standard:	Open Compute Project Mezzanine Card hardware Specification 0.3 PCI-Express Base Specification Revision 2.0 (5GT/s)
Form Factor:	Open Compute Project Mezzanine adapter
PCI Express Card Type:	X4 Lane
PCI Express Voltage	+12V +- 8%
PCI Connector:	FCI 61083-124402LT or equivalent mounted on the mezzanine adapter
Controller:	Intel I350BT2
I/O:	Dual RJ45 located on edge of the board
Power Consumption:	3.36W, 0.28A at 12V: Typical all ports operate at 1000Mbit/s. 2.64 W, 0.22A at 12V: Typical all ports operate at 100Mbit/s. 2.4 W, 0.2 at 12V: Typical all ports operate at 10Mbit/s.

	2.28 W, 0.19A at 12V: Typical No link at all ports
Operating Humidity:	0%–90%, non-condensing
Operating Temperature:	0°C – 50°C (32°F – 122°F)
Storage:	-20°C–65°C (-4°F–149°F)
EMC Certifications:	FCC Part 15, Subpart B Class B Conducted Emissions Radiated Emissions CE EN 55022: 1998 Class B Amendments A1: 2000; A2: 2003 Conducted Emissions Radiated Emissions CE EN 55024: 1998 Amendments A1: 2000; A2: 2003 Immunity for ITE Amendment A1: 2001 CE EN 61000-3-2 2000, Class A Harmonic Current Emissions CE EN 61000 3-3 1995, Amendment A1: 2001 Voltage Fluctuations and Flicker CE IEC 6100-4-2: 1995 ESD Air Discharge 8kV. Contact Discharge 4kV. CE IEC 6100-4-3:1995 Radiated Immunity (80-1000Mhz), 3V/m 80% A.M. by 1kHz CE IEC 6100-4-4:1995 EFT/B: Immunity to electrical fast transients 1kV Power Leads, 0.5Kv Signals Leads CE IEC 6100-4-5:1995 Immunity to conductive surges COM Mode; 2kV, Dif. Mode 1kV CE IEC 6100-4-6:1996 Conducted immunity (0.15-80 MHz) 3VRMS 80% A.M. By 1kHz CE IEC 6100-4-11:1994 Voltage Dips and Short Interruptions V reduc >95%, 30% >95% Duration 0.5per, 25per, 250per
LEDs	
LEDs:	(2) Led's per port Link / Act: Turn on any Link (1000, 100 or 10), Blinks on Activity (green) SPD: Turn on any Speed (Amber)

LEDs location:	LED are integrated on RJ45 connectors
Connectors:	(2) Shielded RJ-45

Order Information

P/N	Description	Notes
OE2G2I35	Dual Port Copper Gigabit Ethernet OCP Mezzanine Adapter	X4 Gen2 , Based on Intel I350AM2, Low-profile. RoHS compliant

Model P/N -LP /-E

1V4